CLAIMS

What is Claimed is:

1. A switched mode power supply comprising:

at least one power switch adapted to convey power between input and output terminals of said power supply; and

a digital controller adapted to control operation of said at least one power switch responsive to an output measurement of said power supply, said digital controller comprising:

an analog-to-digital converter providing a digital error signal representing a voltage difference between said output measurement and a reference value, said analog-to-digital converter further comprises a windowed flash analog-to-digital converter having a transfer function defining a relationship between said voltage difference and corresponding digital values, said transfer function having a substantially linear region at a center of a corresponding error window, said transfer function further comprises a first step size in said center of said error window and at least one additional step size in a peripheral region of said error window, each said at least one additional step size being larger than said first step size;

a digital filter providing a digital control output based on a sum of current and previous error signals and previous control outputs; and

a digital pulse width modulator providing a control signal to said at least one power switch, said control signal having a pulse width corresponding to said digital control output.

2. The power supply of Claim 1, wherein said first step size and said at least one additional step size each reflect a linear relationship between said voltage difference and said corresponding digital values.

3. The power supply of Claim 1, wherein said first step size reflects a linear relationship between said voltage difference and said corresponding digital values, and said at least one additional step size reflects a non-linear relationship between said voltage difference and said corresponding digital values.

4. The power supply of Claim 1, wherein said windowed flash analog-to-digital converter provides a HIGH signal reflecting a negative saturation of said analog-to-digital converter and a LOW signal reflecting a positive saturation of said analog-to-digital converter.

5. The power supply of Claim 1, wherein said digital filter further comprises an infinite impulse response filter.

6. The power supply of Claim 5, wherein said infinite impulse response filter provides the following transfer function G(z):

$$G(z) = \frac{PWM(z)}{VEd(z)} = \frac{C_0 + C_1 \cdot z^{-1} + C_2 \cdot z^{-2} + ... + C_n \cdot z^{-n}}{1 - B_1 \cdot z^{-1} - B_2 \cdot z^{-2} - ... - B_n \cdot z^{-n}}$$

wherein PWM(z) is the digital control output, VEd(z) is the error signal, $C_0 \ldots C_n$ are input side coefficients, and $B_1 \ldots B_n$ are output side coefficients.

7. The power supply of Claim 1, wherein said digital filter further comprises a range limiter adapted to clip said digital control output if upper or lower range limits are reached.

8. The power supply of Claim 7, wherein said range limiter provides a limit signal to said error controller if said upper or lower range limits are reached.

9. The power supply of Claim 1, wherein said digital controller further comprises a multiplexer coupled to said error controller and to said digital filter, said error controller providing an alternative digital control output to said multiplexer that passes to said digital pulse width modulator upon said error condition.

10. The power supply of Claim 1, further comprising an error controller adapted to modify operation of said digital filter upon an error condition.

11. The power supply of Claim 10, wherein said error controller is further adapted to preset at least one of said previous error signals with predetermined values upon said error condition.

12. The power supply of Claim 10, wherein said error controller is further adapted to preset at least one of said previous control outputs with predetermined values upon said error condition.

13. The power supply of Claim 10, wherein said error controller is further adapted to reset at least one of said previous error signals to initial values upon said error condition.

14. The power supply of Claim 10, wherein said error controller is further adapted to reset at least one of said previous control outputs to initial values upon said error condition.

15. The power supply of Claim 10, wherein said error condition further comprises a saturation of said analog-to-digital converter.

16. The power supply of Claim 10, wherein said error condition further comprises a mathematical overflow of said digital filter.

17. A method of controlling a switched mode power supply comprising at least one power switch adapted to convey power between input and output terminals of said power supply, said method comprising:

receiving an output measurement of said power supply;

sampling said output measurement to provide a digital error signal representing a voltage difference between said output measurement and a reference value in accordance with a transfer function defining a relationship between said voltage difference and corresponding digital values, said transfer function having a substantially linear region at a center of a corresponding error window, said transfer function further comprising a first step size in said center of said error window and at least one other step size in a peripheral region of said error window, each said at least one other step size being larger than said first step size;

filtering said digital error signal to provide a digital control output based on a sum of current and previous error signals and previous control outputs; and

providing a control signal to said at least one power switch, said control signal having a pulse width corresponding to said digital control output.

18. The method of Claim 17, wherein said sampling step further comprises providing a HIGH signal reflecting a negative saturation state and a LOW signal reflecting a positive saturation state.

19. The method of Claim 17, wherein filtering step further comprises filtering said digital error signal using an infinite impulse response filter.

20. The method of Claim 17, wherein said filtering step further comprises filtering said digital error signal in accordance with the following transfer function G(z):

$$G(z) = \frac{PWM(z)}{VEd(z)} = \frac{C_0 + C_1 \cdot z^{-1} + C_2 \cdot z^{-2} + \ldots + C_n \cdot z^{-n}}{1 - B_1 \cdot z^{-1} - B_2 \cdot z^{-2} - \ldots - B_n \cdot z^{-n}}$$

wherein PWM(z) is the digital control output, VEd(z) is the error signal, $C_0 \ldots C_n$ are input side coefficients, and $B_1 \ldots B_n$ are output side coefficients.

21. The method of Claim 17, wherein said filtering step further comprises clipping said digital control output if upper or lower range limits are reached.

22. The method of Claim 21, wherein said filtering step further comprises providing a limit signal indicating that said upper or lower range limit is reached.

23. The method of Claim 17, further comprising providing an alternative digital control output upon said error condition.

24. The method of Claim 17, wherein said first step size and said at least one other step size each reflect a linear relationship between said voltage difference and said corresponding digital values.

25. The method of Claim 17, wherein said first step size reflects a linear relationship between said voltage difference and said corresponding digital values, and said at least one other step size reflects a non-linear relationship between said voltage difference and said corresponding digital values.